Backend DSP Functional Description

Wisconsin SCT/pixel ROD Group:

K. Dao
D. Fasching
R. Jared
J. Joseph
M. Nagel
L. Stromburg
L. Tomasek

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- The ROD layout supports 5 DSPs.
  - One master DSP in the ROD controller
    - TI TMS320C6201, 200 MHz
    - Host Port Interface: 16 bits data, 16 bits address
    - External Memory Interface: 32 bits data, 16 bits address
    - 2 serial links (L1A input from fast command logic)
    - internal program and data memory, 512 Kbit each
  - Backend slave DSPs on the Router
    - TI TMS320C6701, 167 MHz
    - Host Port Interface: 16 bits data, 16 bits address
    - External Memory Interface: 32 bits data, 26 bits address
    - 2 serial links
    - internal program and data memory, 512 Kbit each
- Initially, 2 of the backend DSPs will be loaded on the ROD.
- Each of the DSPs has 16 MBytes of SDRAM attached.
- Here we will discuss the functions of the backend DSPs.

Run-Time Functions

- DSP module 0: Monitoring, Error Scaling
  - Occupancy histogram accumulation; assume 2 bytes per detector element
    - 96 link SCT ROD requires 260 KBytes
    - 28 link pixel ROD requires 4 MBytes
    - Allows keeping a reference occupancy map to check data quality locally
    - Persistent problems can be communicated to the ROD controller.
  - Error Scaling
    - A partition of SDRAM or local DSP memory can be used to scale data errors on a link-by-link basis
    - link-by-link errors
      - timeout
      - preamble error
      - BCID error
      - L1ID error
      - bit error
      - bad hit data
      - encoded error from FE chip
      - header only mode
      - data overflow
      - trailer bit error
    - event-by-event errors

Run-Time Functions

- DSP module 1: Error Diagnosis and Recovery
  - Events can be trapped by this DSP based on error bits and error conditions.
  - For some persistent errors this DSP will execute algorithms to determine the cause of the error.
  - Three courses of action are then possible:
    - Ignore the error, allowing error flagged events to continue to being transmitted.
    - Interrupt the RCC which can determine what action needs to be taken, if any.
    - Attempt local error recovery.
  - There are two types of error for which the capability to implement local correction algorithms has been engineered into the ROD.
    - Event synchronization errors. The dynamic readout mask to the formatters and the L1ID offset modifier FIFO to the event fragment builder allow the ROD to recover locally from most conditions which will lead to a loss of synchronization. Persistent BCID errors on a single link indicate a loss of synchronization and dictate the setting of the dynamic mask. The presence or absence of a L1ID error at the same time determines the setting of the L1ID offset modifier.
    - Persistent event timeouts or data overflow errors on a link may indicate that that link requires resetting. The dual FE command stream masks allows this to be done without interrupting data taking. The large SDRAM in the ROD Controller is sufficient to store the configuration information for all modules controlled by a ROD.

Calibration

- The backend has 32 MBytes available to store calibration data. There are two possibilities for storing calibration data in the backends.
  - Write the data words sequentially into one or the other memory as they arrive.
  - Histogram the data by detector element number and possibly some scan index.
- In a histogram mode, 32 MBytes allows a 24 bit address space with 2 bytes of data per location.
  - Every detector element in a 48 module (96 data link) SCT ROD can be identified by 17 bits. The data for a 128 point scan with 64 K pulses per point can be histogrammed on the ROD. Larger scans would require intermediate data transfers.
  - 21 bits are required to identify every detector element in a 28 module pixel ROD. Any reasonable scan of the entire space controlled by the ROD therefore requires intermediate data transfers off the ROD. Such large scans may be part of routine system maintenance.
- Initially the software to analyze calibration data will reside on the ROD Crate Controller.

- This software will migrate to the backend DSPs as seen fit. In cases where all of the histogram data does not fit in the available memory, this implies that full scan histograms would need to be collected on a subset of channels and then fit, and the results would have to be transferred off the ROD before starting the next subset of channels.

Work in progress

- Work on the DSP software is just beginning.
  - At LBNL we have had a 6201 DSP evaluation module (PCI bus card with a DSP and some memories) available since early in the summer. With this we began to understand the properties of the DMA engine. (student Phi Dao)
  - We have recently acquired an EVM for the 6701.
  - Iowa State has recently joined the ROD effort. Tom Meyer has been at LBNL for the past week and will return for 2 to 3 weeks in January. Iowa State has also acquired a 6701 EVM.
- There is clearly a lot of work to do on the backend DSP software and the communication protocol between the backends and the ROD controller.
- The hardware design allows for some very powerful features to be implemented and the software has to be designed carefully if we are to be able to take advantage of the features designed into the board.
- There are two groups with the tools necessary to do real work on this software and on understanding the DSPs. Contact between these groups is off to a good start.